

**Version with markings to show changes made**

**In The Title**

Please delete the present title and insert therefore the following new title:

**MEMORY SHARING ARRANGEMENT FOR AN INTEGRATED  
MULTIPROCESSOR SYSTEM**

**In the Claims**

- 1 **17. (New) An electronic product, comprising:**
- 2 **a first processor coupled to an instruction cache and to a data cache;**
- 3 **a first bus coupled to the instruction cache and to the data cache;**
- 4 **a first memory coupled to the first bus;**
- 5 **a second processor coupled to a second bus;**
- 6 **a first bus bridge coupled to the first bus and to the second bus, the first**
- 7 **bus bridge providing a path for transferring data between the first memory and**
- 8 **the second processor;**
- 9 **a second memory coupled to the first bus;**
- 10 **a second bus bridge coupled to the second bus and a third bus, the third**
- 11 **bus providing a data pathway within the first processor, the second bus bridge**
- 12 **providing a path for transferring data between the second memory and the third**
- 13 **bus of the first processor; and**
- 14 **a direct memory access (DMA) controller coupled to the second bus, the**
- 15 **DMA controller configured to manage a transfer of data between the second**
- 16 **memory and the second bus bridge;**